

SITAO HUANG

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EDUCATION

- May, 2014 – present **Ph.D. candidate** in Department of Electrical and Computer Engineering, UIUC.
M. S. in Electrical and Computer Engineering, UIUC.
Supervised by Prof. Deming Chen and Prof. Wen-Mei W. Hwu.
- Aug., 2010 – Jun., 2014 **B. S.** in Electronic and Information Science, Tsinghua University.

INTERNSHIPS

- May, 2018 – Aug., 2018 **Microsoft Research** – AI Infrastructures *Sunnyvale, California, USA*
- May, 2017 – Aug., 2017 **Microsoft Research** – Deep Learning Group *Redmond, Washington, USA*
- May, 2016 – Aug., 2016 **Synopsys** – ZeBu Team, Verification Group *Mountain View, California, USA*
- Dec., 2013 – May, 2014 **Microsoft Research Asia** – System Algorithm Group *Beijing, China*

PUBLICATIONS

- **Sitao Huang**, Mohamed El-Hadedy, Cong Hao, Qin Li, Vikram S. Mailthody, Ketan Date, Jinjun Xiong, Deming Chen, Rakesh Nagi, Wen-mei Hwu. Triangle Counting and Truss Decomposition using FPGA. *IEEE High Performance Extreme Computing Conference Graph Challenge (HPEC 2018)*.
- Joao Ambrosi, Rodrigo Antunes, Aayush Ankit, Sai Rahul Chalamalasetti, Soumitra Chatterjee, Izzat El Hajj, Guilherme Fachini, Paolo Faraboschi, Martin Foltin, **Sitao Huang**, Wen-mei Hwu, et al (alphabetical order). Hardware-Software Co-Design for an Analog-Digital Accelerator for Machine Learning. *IEEE International Conference on Rebooting Computing (ICRC 2018)*.
- Po-Sen Huang, Chong Wang, **Sitao Huang**, Dengyong Zhou, Li Deng. Towards Neural Phrase-based Machine Translation. *The 6th International Conference on Learning Representations (ICLR 2018)*.
- Li-Wen Chang, Juan Gómez Luna, Izzat El Hajj, **Sitao Huang**, Deming Chen and Wen-Mei Hwu. Collaborative Computing for Heterogeneous Integrated Systems. Proceedings of *the 8th ACM/SPEC on International Conference on Performance Engineering (ICPE 2017)*, pp. 385-388, 2017.
- **Sitao Huang**, Gowthami Jayashri Manikandan, Anand Ramachandran, Kyle Rupnow, Wen-Mei Hwu, Deming Chen. Hardware Acceleration of the Pair-HMM Algorithm for DNA Variant Calling. Proceedings of *the 25th ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (FPGA 2017)*, pp. 275-284, 2017.
- Yuliang Sun, Zilong Wang, **Sitao Huang**, Lanjun Wang, Yu Wang, Rong Luo, and Huazhong Yang. Accelerating Frequent Item Counting with FPGA. Proceedings of *the 22nd ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (FPGA 2014)*, pp. 109-112, 2014.
- **Sitao Huang**, Guohao Dai, Yuliang Sun, Zilong Wang, Yu Wang and Huazhong Yang. DTW-Based Subsequence Similarity Search on AMD Heterogeneous Computing Platform. Proceedings of *the 15th IEEE International Conference on High Performance Computing and Communications (HPCC 2013)*, pp.1054–1063, 2013.
- Zilong Wang, **Sitao Huang**, Lanjun Wang, Hao Li, Yu Wang and Huazhong Yang. Accelerating Subsequence Similarity Search Based on Dynamic Time Warping Distance with FPGA. Proceedings of *the 21st ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (FPGA 2013)*, pp. 53-62, 2013.

SELETED RESEARCH PROJECTS

- **Deep Neural Network Training on Memristor-based Accelerator**
IMPACT Research Group, Hewlett Packard Labs *Jan., 2018 – present*
- **Real-Time DNN-based Object Detection on Embedded FPGA and GPU Platforms**
ES-CAD Research Group and IMPACT Research Group, ECE, UIUC *Nov., 2017 – present*
- **Accelerating Neural Phrase-based Machine Translation on Multi-GPUs**

- Microsoft Research, Redmond, Washington, USA* *May., 2017 – Aug., 2017*
- Achieve effective acceleration over GPU-enabled Torch implementation.
 - **Tangram: A High-Level Language for Heterogeneous Computing**
IMPACT Research Group, ECE, UIUC *Feb., 2017 – present*
 - High-level performance portable language for CPUs, GPUs, etc.; Working on CUDA and OpenMP code generation.
 - **Collaborative Computing on CPU-FPGA and CPU-GPU Platforms**
IMPACT Research Group and ES-CAD Research Group, ECE, UIUC *Nov., 2016 – present*
 - Improve system performance with tight collaboration of CPU and accelerators.
 - **Pipeline Optimization in High Level Synthesis Targeting Low-Power Design**
ES-CAD Research Group and IMPACT Research Group, ECE, UIUC *Jan., 2016 – May, 2016*
 - **Hardware Acceleration of the Pair-HMM algorithm for DNA Variant Calling**
ES-CAD Research Group and IMPACT Research Group, ECE, UIUC *Nov., 2015 – Sept., 2016*
 - Achieve best performance among published hardware implementations.
 - **Clock Tree Optimization for FPGA-Based Emulation System**
Synopsys Inc., Mountain View, California, USA *May, 2016 – Aug., 2016*
 - **HOCL: A New Hardware Compilation Flow with OpenCL**
ES-CAD Research Group and IMPACT Research Group, ECE, UIUC *Aug., 2014 – May, 2015*
 - **Thread Scheduling and Power Management Related Optimization in Multi-Core Systems**
System Algorithm Group, Microsoft Research Asia, Beijing, China *Dec., 2013 – May, 2014*
 - Intern, mentored by Dr. Thomas Moscibroda.
 - **System-Level Design Space Exploration Automation for Subsequence Similarity Search**
VAST Lab, Computer Science Department, UCLA *Jul., 2013 – Sept., 2013*
 - Internship, mentored by Prof. Jason Cong and Dr. Peng Zhang. Established automated Design Space Exploration (DSE) flow, achieved effective speedup over the best software implementation while guaranteeing QoS.
 - **Subsequence Similarity Search Acceleration Based on Dynamic Time Warping (DTW) Distance on Heterogeneous Computing Platform**
NICS Lab, Dept. of E.E., Tsinghua University *Jan., 2013 – Jun., 2013*
 - **Subsequence Similarity Search Acceleration Based on Dynamic Time Warping Distance with FPGA**
NICS Lab, Dept. of E.E., Tsinghua University and IBM Research China *Jun., 2012 – Oct., 2012*

SELECTED COURSES

Introduction to VLSI System Design; System-On-Chip Design; Manycore Parallel Algorithms; Algorithms; Distributed Algorithms; Computer Architecture; Parallel Computer Architecture; Programming Languages & Compilers; Compiler Construction; Machine Learning; Random Processes; MDPs, Reinforcement Learning

HONORS AND POSITIONS

- Student Innovation Award in IEEE HPEC Graph Challenge 2018.
- Third place (out of 61 teams) in System Design Contest at Design Automation Conference 2018 (DAC 2018).
- UIUC ECE Rambus Computer Engineering Fellowship. 2018 – 2019.
- Academic Innovation Scholarship Winner in the Department of E.E., Tsinghua University, 2013.
- Session Chair in the 15th IEEE Intl. Conf. on High Performance Computing and Communications (IEEE HPCC 2013).
- First prize in the 28th National Competition in Physics for University Students, Non-Physics Major.
- Third prize in the 31st “Challenge Cup” Competition of Science & Technology in Tsinghua University.
- First prize in the 26th Chinese Physics Olympiad (CPhO) in Provinces.

SKILLS

Programming Languages: Proficient in using C/C++, Python, JavaScript, Java, OCaml, MATLAB, Verilog, etc.

Softwares/Frameworks: LLVM, CUDA, OpenCL, Quartus II/Prime, Vivado, ModelSim, Visual Studio, LaTeX, etc.