# SITAO HUANG

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## EDUCATION

- Aug., 2014 – present **Department of Electrical and Computer Engineering, UIUC.** GPA: 3.84/4.00. *(MS/PhD)*
  Supervised by **Prof. Deming Chen** and **Prof. Wen-Mei W. Hwu**.
- Jun., 2011 – Jun., 2014 **Department of Electronic Engineering, Tsinghua University**. GPA: 3.7/4.0. *(BS)*
- Aug., 2010 – Jun., 2011 **Department of Hydraulic Engineering, Tsinghua University**. GPA: 3.8/4.0.

## HONORS AND POSITIONS

- Academic Innovation Scholarship Winner in the Department of E.E., Tsinghua University, 2013.
- **Session Chair** in the 15th IEEE International Conference on High Performance Computing and Communications (IEEE HPCC 2013).
- **First prize** in the 28th National Competition in Physics for University Students, Non-Physics Major.
- **Third prize** in the 31st "Challenge Cup" Competition of Science & Technology in Tsinghua University.
- **First prize** in the 26th Chinese Physics Olympiad (CPhO) in Provinces, recommended to Tsinghua University.

## PUBLICATIONS

- Li-Wen Chang, Juan Gómez Luna, Izzat El Hajj, **Sitao Huang**, Deming Chen and Wen-Mei Hwu. Collaborative Computing for Heterogeneous Integrated Systems. (***ICPE 2017***, to appear)
- **Sitao Huang**, Gowthami Jayashri Manikandan, Anand Ramachandran, Kyle Rupnow, Wen-Mei Hwu, Deming Chen. Hardware Acceleration of the Pair-HMM Algorithm for DNA Variant Calling. *Proceedings of the 25th ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (**FPGA 2017**)*, pp. 275-284, 2017.
- Yuliang Sun, Zilong Wang, **Sitao Huang**, Lanjun Wang, Yu Wang, Rong Luo, and Huazhong Yang. Accelerating Frequent Item Counting with FPGA. *Proceedings of the 22nd ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (**FPGA 2014**)*, pp. 109-112, 2014.
- **Sitao Huang**, Guohao Dai, Yuliang Sun, Zilong Wang, Yu Wang and Huazhong Yang. DTW-Based Subsequence Similarity Search on AMD Heterogeneous Computing Platform. *Proceedings of the 15th IEEE International Conference on High Performance Computing and Communications (**HPCC 2013**)*, pp.1054–1063, 2013.
- Zilong Wang, **Sitao Huang**, Lanjun Wang, Hao Li, Yu Wang and Huazhong Yang. Accelerating Subsequence Similarity Search Based on Dynamic Time Warping Distance with FPGA. *Proceedings of the 21st ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (**FPGA 2013**)*, pp. 53-62, 2013.

## RESEARCH EXPERIENCE

- **Pipeline Optimization in High Level Synthesis Targeting Low-Power Design**
  *ES-CAD Group and IMPACT Group, ECE, UIUC* *Jan., 2016 – present*
  - Power-aware high level synthesis flow based on pipeline optimization.
- **Hardware Acceleration of the Pair-HMM algorithm for DNA Variant Calling**
  *ES-CAD Group and IMPACT Group, ECE, UIUC* *Nov., 2015 – Sept., 2016*
  - Achieve best performance among published hardware implementations.
  - Paper accepted by **FPGA 2017**.
- **Clock Tree Optimization for FPGA-Based Emulation System**
  *Synopsys Inc.* *May, 2016 – Aug., 2016*
  - Intern. This work is a part of Synopsys ZeBu Emulation System project.
- **HOCL: A New Hardware Compilation Flow with OpenCL**
  *ES-CAD Group and IMPACT Group, ECE, UIUC* *Aug., 2014 – May, 2015*

- **Thread Scheduling and Power Management Related Optimization in Multi-Core Systems**
  *System Algorithm Group, Microsoft Research Asia* *Dec., 2013 – May, 2014*
  - Intern, mentored by Dr. Thomas Moscibroda.
- **System-Level Design Space Exploration Automation for Subsequence Similarity Search**
  *VAST Lab, Computer Science Department, UCLA* *Jul., 2013 – Sept., 2013*
  - Summer internship in UCLA VAST Lab, mentored by Prof. Jason Cong and Dr. Peng Zhang.
  - Apply system-level synthesis method to subsequence similarity search problem.
  - Established an automated Design Space Exploration (DSE) flow for the design parameters in the system.
  - Achieved efficient acceleration compared to best software implementation while guaranteeing effective QoS.
- **Subsequence Similarity Search Acceleration Based on Dynamic Time Warping (DTW) Distance on Heterogeneous Computing Platform**
  *NICS Lab, Dept. of E.E., Tsinghua University, Team Leader* *Jan., 2013 – Jun., 2013*
  - Achieved **about two orders** of magnitude speedup over best software implementation, and several times speedup over the other GPU implementations and even some FPGA implementations.
  - Paper accepted by **HPCC 2013**.
- **Subsequence Similarity Search Acceleration Based on Dynamic Time Warping Distance with FPGA**
  *NICS Lab, Dept. of E.E., Tsinghua University and IBM Research China* *Jun., 2012 – Oct., 2012*
  - Achieved **two orders** of magnitude speedup compared with previous FPGA implementations and **more than two orders** compared with best software implementation.
  - Paper accepted by **FPGA 2013**.
- **Hardware Implementation of Handshake Join Structure**
  *NICS Lab, Dept. of E.E., Tsinghua University and IBM Research China* *Apr., 2012 – Jun., 2012*
  - Handshake join is one of hardware structures implementing stream join operation in data mining tasks.
  - In charge of the design of interpolation module; designed an interpolation module that can realize interpolation of any given rational fraction with a high throughput.
- **Hardware Implementation of Apriori Algorithm**
  *NICS Lab, Dept. of E.E., Tsinghua University and IBM Research China* *Feb., 2012 – Apr., 2012*
  - *Apriori* is one of frequent itemsets algorithms, which is a common operation in data mining tasks.
  - In charge of algorithms survey and a part of modules implementation.
- **Real-time Image Processing Hardware Prototype System**
  *NICS Lab, Dept. of E.E., Tsinghua University* *Sept., 2011 – Feb., 2012*
  - In charge of the development of several basic image processing modules, such as Sobel edge detector, Auto-threshold module, etc. On a Stratix IV GX FPGA board.

## COURSE PROJECTS

- Nov., 2013 **A Webpage Keyword Search System based on DSP** (TCP/IP, HTTP, embedded OS involved)
- Jul., 2013 **A Document Relevance Analyzer** (in Python; using several data mining algorithms)
- Nov., 2012 **A Network TCP/IP Package Traffic Analyzer** (in Python)
- Jul., 2012 **MIPS 32 bits Microprocessor Implemented on FPGA**
- Jul., 2012 **A Color Histogram Based Face Detector** (in MATLAB scripts)
- Jun., 2012 **A Ultrasonic Distance Measurement Module** (a mixed-signal circuit design)
- May, 2012 **A SPI Controller** (in Verilog; using NCLaunch, Design Vision and Encounter)
- Aug., 2011 **A Web Crawler and An Offline Dictionary** (in Python)

## SKILLS

**Programming Languages:** Proficient in using C/C++, Java, Python, JavaScript, OCaml, MATLAB, Verilog, etc.

**Softwares/Frameworks:** LLVM, CUDA, OpenCL, Quartus II/Prime, Vivado, ModelSim, Visual Studio, LaTeX, etc.